



2N7002KTB

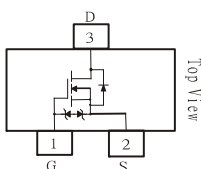
60V N-Channel Enhancement Mode MOSFET - ESD Protected

FEATURES

- $R_{DS(ON)}$, $V_{GS}@10V, I_{DS}@500mA=3\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V, I_{DS}@200mA=4\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers : Relays, Displays, Lamps, Solenoids, Memories, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS2.0 (2011/65/EU & 2015/865/EU directive)
- Green molding compound as per IEC61249 Std. . (Halogen Free)

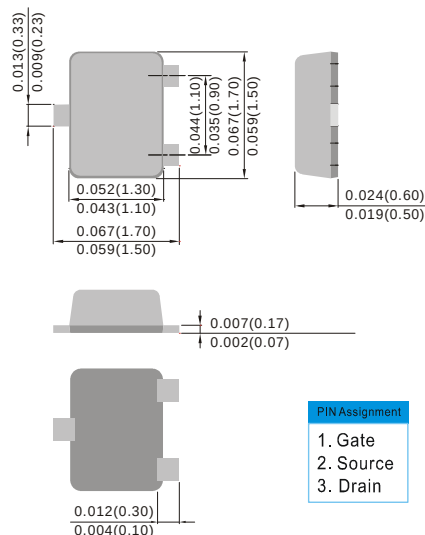
MECHANICAL DATA

- Case: SOT-523 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.00007 ounces, 0.002 grams
- Marking: 27



SOT-523

Unit : inch(mm)



PIN Assignment
1. Gate
2. Source
3. Drain

Maximum RATINGS and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	115	mA
Pulsed Drain Current ¹⁾	I_{DM}	800	mA
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$ 200 $T_A=75^\circ\text{C}$ 150	mW
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^\circ\text{C}$
Junction-to Ambient Thermal Resistance(PCB mounted) ²⁾	$R_{\theta JA}$	883	$^\circ\text{C/W}$

Note:1.Maximum DC current limited by the package

2.Surface mounted on FR4 board, $t \leq 10$ sec

3.Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

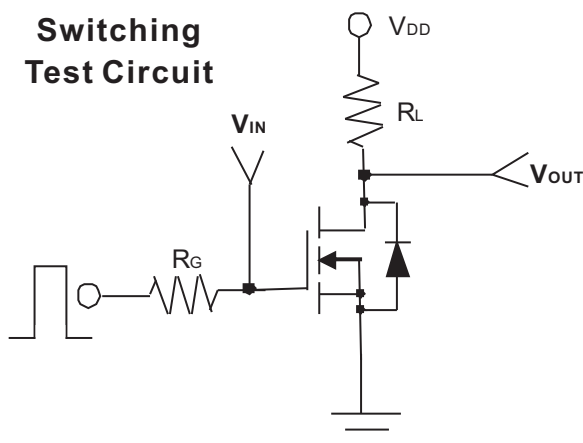


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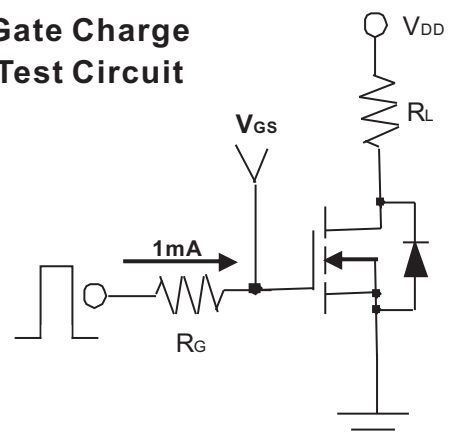
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=10\mu A$	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=200mA$	-	-	4.0	Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	-	3.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate Body Leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 10	μA
Forward Transconductance	g_{fs}	$V_{DS}=15V, I_D=250mA$	100	-	-	mS
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=200mA$ $V_{GS}=4.5V$	-	-	0.8	nC
Turn-On Delay Time	$td_{(on)}$	$V_{DD}=30V, R_L=150\Omega$ $I_D=200mA, V_{GEN}=10V$ $R_G=10\Omega$	-	-	20	ns
Turn-Off Delay Time	$td_{(off)}$		-	-	125	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1.0MHz_z$	-	-	35	pF
Output Capacitance	C_{oss}		-	-	10	
Reverse Transfer Capacitance	C_{rss}		-	-	5	
Source-Drain Diode						
Diode Forward Voltage	V_{SD}	$I_S=200mA, V_{GS}=0V$	-	0.82	1.3	V
Continuous Diode Forward Current	I_s	-	-	-	115	mA
Pulsed Diode Forward Current	I_{sM}	-	-	-	800	mA

Switching Test Circuit



Gate Charge Test Circuit





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Typical Characteristics Curves ($T_A=25^\circ\text{C}$, unless otherwise noted)

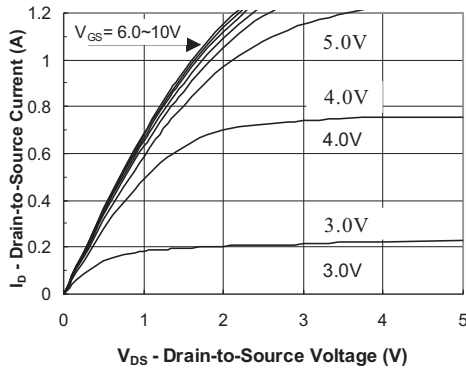


FIG.1- Output Characteristic

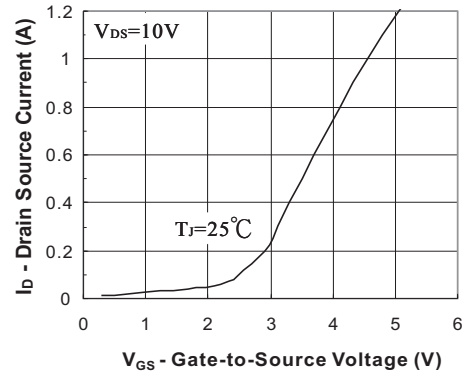


FIG.2- Transfer Characteristic

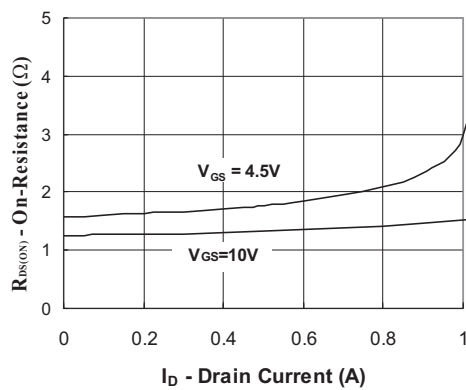


FIG.3- On Resistance vs Drain Current

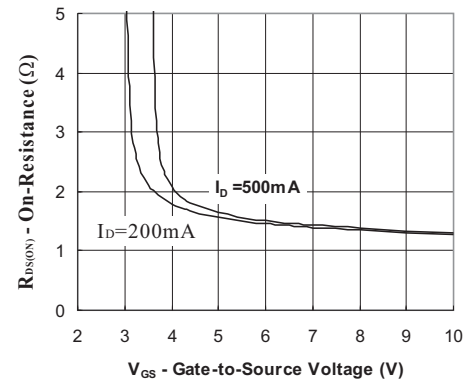


FIG.4- On Resistance vs Gate to Source Voltage

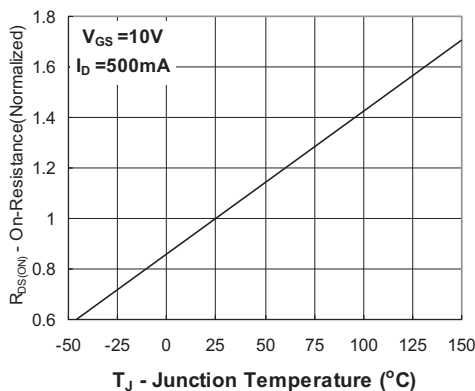


FIG.5- On Resistance vs Junction Temperature



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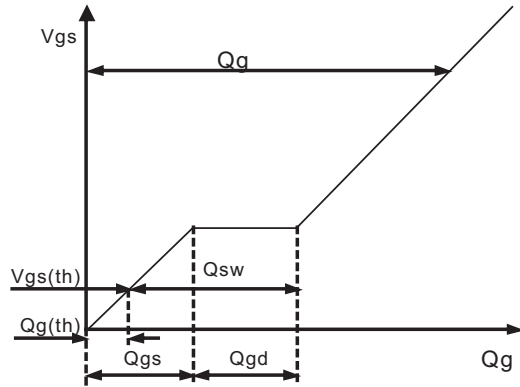


Fig.6 - Gate Charge Waveform

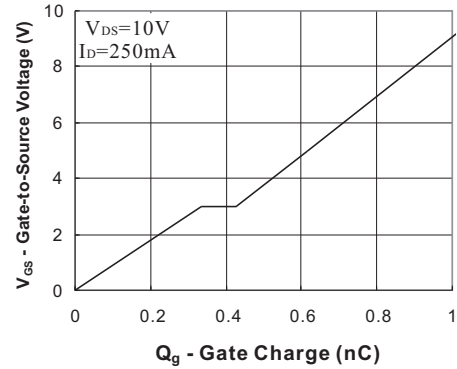


Fig.7 - Gate Charge

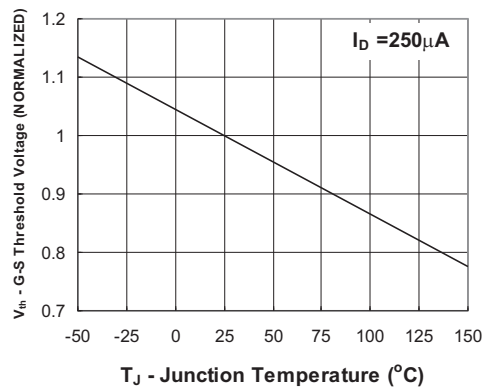


Fig.8 - Threshold Voltage vs Temperature

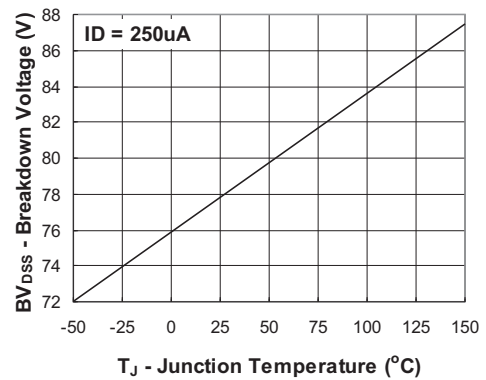


Fig.9 - Breakdown Voltage vs Junction Temperature

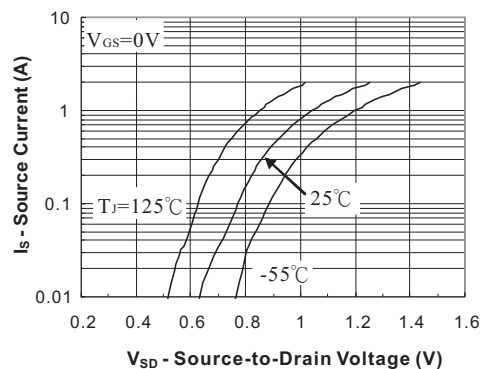


Fig.10 - Source-Drain Diode Forward Voltage